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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
POMPEY, RON EVERETT	
ART UNIT	PAPER NUMBER
2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,361	CHAN ET AL.	
	Examiner	Art Unit	
	Ron E. Pompey	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-5, 9, 14-15, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clark et al. (US 6767793) in view of Fried et al. (USPG 2003/0113970).

Clark discloses the limitations of forming a multiple gate electrode in claims 1, 3-5, 9, 14-15, 17 and 18:

Claims 1: coating a layer of gate electrode material (310, fig. 31) over top and past the opposed sides of a semiconductor device (300 fig. 30) that has been previously coated with a thin film of gate dielectric (320 , fig. 31) (Column 7, lines 43 – 65)

Claim 3: conforming the layer of gate electrode material with a step height increase corresponding to an increased step height of the semiconductor device (though not shown layer 310 will formed conformally like layer 50 in fig.5);

Claim 4: wherein the semiconductor fin comprises a silicon fin (300, fig. 30);

Claim 5: wherein the semiconductor fin comprises a fin of silicon and germanium (300, fig. 30);

Claim 9: wherein, the gate dielectric comprises silicon oxide (320, fig. 31);

Claim 14: wherein, the multiple gate electrode comprises polycrystalline silicon (310, fig. 7; col. 7, lns. 53-54);

Claim 15: wherein, the multiple gate electrode comprises a conductive material(310, fig. 7; col. 7, lns. 53-54);

Claim 17: the semiconductor device having a projecting fin (300, fig. 31) coated with a gate dielectric film over top and opposed sides of the fin (320, fig. 31);

the multiple gate electrode is a portion of the layer of gate electrode material, which has a planarized surface that includes the planar surface of the multiple gate electrode(310, fig. 7; col. 7, lns. 53-54);

providing a semiconductor device(310, fig. 7) over a planar surface that extends from each of opposed sides of the semiconductor device (300, fig. 30);

coating a top and the opposed sides of the semiconductor device (300, fig. 31) with a thin film gate dielectric (320, fig. 31);

coating a layer of gate electrode (310, fig. 7) material over the semiconductor device (300, fig. 30) and the planar surface (top of 300);

and planarizing the layer of gate electrode material to produce a substantially planar surface formed only of the gate electrode material prior to patterning the gate electrode (310, fig. 7; col. 7, lns. 53-56);

Claim 18: wherein the semiconductor device comprises a semiconductor fin with a planar top surface.

3. Clark does not disclose the limitation(s) of claims 1 and 17:

Claims 1 and 17: planarizing the layer of gate electrode material to produce a substantially planar surface formed only of the gate electrode material disposed atop the semiconductor device and extending past each of the opposed sides, prior to patterning the gate electrode material to form a discrete multiple gate electrode on the semiconductor device;

a multiple gate electrode on each of the opposed sides of the fin, the multiple gate electrode formed of a layer of gate electrode material and having a substantially planar surface disposed atop the gate dielectric film formed over the top of the fin and extending past each of the opposed sides of the fin.

the substantially planar surface having the same height at locations superjacent the semiconductor device and at locations distal the semiconductor device.

a. However, Fried discloses:

Claims 1 and 17: planarizing the layer of gate electrode material (32, fig. 5B) to produce a substantially planar surface formed only of the gate electrode material disposed atop the semiconductor device and extending past each of the opposed sides, prior to patterning the gate electrode material to form a discrete multiple gate electrode on the semiconductor device ([0033]);

the substantially planar surface (top of 32, fig. 5B) having the same height at locations superjacent the semiconductor device and at locations distal the semiconductor device ([0033]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the planarization of the gate material of Clark with the

planarization method of the gate material taught by Fried, because Fried discloses the planarization method that will allow for gate formations on the top and sides and therefore increase scalability of the device.

4. Claims 2, 6-8, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clark et al. (US 6767793) in view of Fried et al. (USPG 2003/0113970) as applied to claim 1 and 17 above, and further view of Kinsbron et al. (US 4432132).

Clark in view of Fried, as indicated above, discloses all the features of the claims except the method of:

Claim 2, 6-8, and 17: applying a photoresist mask of substantially uniform thickness on the planar top surface of the planarized gate electrode material;

patterning the photoresist mask to cover a corresponding pattern of the discrete multiple gate electrode;

etching the gate electrode material that is uncovered by the photoresist mask to form the discrete multiple gate electrode.

b. However Kinsborn discloses:

applying a photoresist mask (14, fig. 1) of substantially uniform thickness on the planar top surface of gate electrode material (12, fig. 1);

patterning the photoresist mask (14, fig. 1) to cover a corresponding pattern of the discrete multiple gate electrode (col. 3, lns. 21-40);

etching the gate electrode material (12, fig. 2) that is uncovered by the photoresist mask to form the gate electrode (col. 3, lns. 46-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the patterning of the gate material in Clark and Fried by using the explicit steps to pattern a gate material as taught in Kinsborn, because Kinsborn discloses a conventional patterning technique in greater detail than Clark and Fried.

5. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clark et al. (US 6,767,793) in view of Fried et al. (USPG 2003/0113970) as applied to claim 1 above, and further view of Fried et al. (US 6657252).

Clark in view of Fried, as indicated above, discloses all the features of the claims except the method of:

Claims 10-13: wherein, the gate dielectric comprises silicon oxynitride, a high permittivity material, comprising a permittivity greater than 5 and a thickness in the range of 3 and 100 Angstroms

c. However, Fried discloses:

the various types of gate dielectric material including silicon oxynitride, a high permittivity material, comprising a permittivity greater than 5 and a thickness in the range of 3 and 100 Angstroms (a high dielectric formed to 750-800 angstroms will have a effective electric thickness in the range of 3-100 angstroms) (col. 5, lns 25-32).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the gate oxide in Clark and Fried, with a one comprising a permittivity greater than 5 and a thickness in the range of 3 and 100 Angstroms as taught by Fried, because Fried discloses that the various types of gate dielectric

materials were conventional gate dielectric material used in the art and it would have been a matter of design choice as to which material to use. Additionally, with oxide of high permittivity you can physically grow the oxide thicker and have a electric effective thickness less, which improves hot carrier effects.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clark et al. (US 6,767,793) in view of Fried et al. (USPG 2003/0113970) as applied to claim 1 above, and further view of Achuthan et al. (US 6767793).

Clark in view of Fried, as indicated above, discloses all the features of the claims except the method of:

Claim 16: wherein, the multiple gate electrode comprises a metal material

d. However, Achuthan discloses:

wherein, the multiple gate electrode comprises a metal material(col. 3, lns. 54-58).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the gate material of Clark or Fried with the gate material taught by Achuthan, because Achuthan discloses the metals are art recognized equivalent materials to use to form gates.

Response to Arguments

1. Applicant's arguments, filed 4/11/07, with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E. Pompey whose telephone number is (571) 272-1680. The examiner can normally be reached on 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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5/14/07

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